IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (previously presented) In a microelectronic device, a structure on a substrate comprising:

a diffusion barrier layer disposed above and on the substrate, the diffusion barrier layer having a first thickness and a first dielectric constant, wherein the first thickness comprises a range from about one atomic monolayer to about 1000 angstroms;

an etch stop layer above and on the diffusion barrier layer, the etch stop layer having a second thickness, and a second dielectric constant; and

an interlayer dielectric (ILD) layer disposed above and on the etch stop layer, wherein the structure has an effective dielectric constant in a range less than about 3.

2. (canceled)

3. (original) The structure according to claim 1, wherein the diffusion barrier layer comprises an organic composition and wherein the etch stop layer comprises an inorganic composition.

4. (original) The structure according to claim 1, wherein the diffusion barrier layer is selected from arylene, parylene, and arylene ether polymers, and fluorinated polyimides.

5. (original) The structure according to claim 1, wherein the diffusion barrier layer comprises an inorganic composition and wherein the etch stop layer comprises an organic composition.

6. (original) The structure according to claim 1, wherein the etch stop layer comprises an organic composition and wherein the diffusion barrier layer is selected from silicon nitride, silicon oxide, silicon oxynitride, aluminum oxide, aluminum nitride, aluminum oxynitride, beryllium oxide, beryllium nitride, beryllium oxynitride, boron oxide, boron nitride, boron oxynitride, cerium oxide, cerium nitride, cerium oxynitride, yttrium oxide, yttrium nitride, yttrium oxynitride, carbon-doped oxide, carbon nitride, carbon oxynitride, a ceramic dielectric, and combinations thereof.

7. (original) The structure according to claim 1, further comprising:

an electrically conductive trace disposed in the substrate; and

a contact disposed in a recess that extends through the ILD layer, the etch stop layer, and the diffusion barrier layer, and wherein the contact makes an electrical connection to the trace.

8. (original) The structure according to claim 1, further comprising:

an electrically conductive trace disposed in the substrate; and

a contact disposed in a recess that extends through the ILD layer, the etch stop layer, and the diffusion barrier layer, and wherein the contact makes an electrical connection to the trace, wherein the contact is a single-damascene contact article.

9. (previously presented) In a microelectronic device, a structure comprising:

a substrate having an upper surface;

an electrically conductive trace in the substrate;

a diffusion barrier layer disposed above and on the substrate and the trace, wherein the diffusion barrier layer comprises a thickness in a range from about one atomic monolayer to about 1000 angstroms;

an etch stop layer above and on the diffusion barrier layer; and

an ILD layer disposed above and on the etch stop layer, wherein the diffusion barrier layer and the etch stop layer are mutually exclusively selected from either an organic composition or an inorganic composition.

10. (original) The structure according to claim 9, wherein the trace surface is coplanar to the upper surface.

11. (canceled)

12. (original) The structure according to claim 9, wherein the ILD layer, the diffusion barrier layer, and the etch stop layer have an effective dielectric coefficient less than about 3.

13. (original) The structure according to claim 9, wherein the ILD layer, the diffusion barrier layer, and the etch stop layer have an effective dielectric coefficient of about 2.8.

14. (original) The structure according to claim 9, wherein the ILD layer, the diffusion barrier layer, and the etch stop layer have an effective dielectric coefficient in a range from about 2.6 to about 2.8.

15. (canceled)

16. (previously presented) An article of manufacture comprising:

a semiconductor substrate;

a first dielectric layer disposed on the semiconductor substrate, wherein the first dielectric layer comprises a thickness in a range from about one atomic monolayer to about 1000 angstroms;

an etch stop layer disposed above and on the first dielectric layer;

an interlayer dielectric (ILD) disposed on the etch stop layer; and

a conductive damascene article, wherein the conductive damascene article is in contact with the substrate, the first dielectric layer, the etch stop layer, and the ILD layer;

and wherein the first dielectric layer is an inorganic composition and comprises a material selected to be a diffusion barrier to prevent diffusion of material of the conductive damascene article into the substrate, and wherein the etch stop layer is an organic composition.

17. (original) The article of claim 16, wherein the first dielectric layer is selected from silicon nitride, silicon oxide, silicon oxynitride, aluminum oxide, aluminum nitride, aluminum oxynitride, beryllium oxide, beryllium nitride, beryllium oxynitride, boron oxide, boron nitride, boron oxynitride, cerium oxide, cerium nitride, cerium oxynitride, yttrium

oxide, yttrium nitride, yttrium oxynitride, carbon-doped oxide, carbon nitride, carbon oxynitride, a ceramic dielectric, and combinations thereof.

18. (previously presented) The article of claim 16, wherein the etch stop layer is selected from arylene, parylene, and arylene ether polymers, and fluorinated polyimides.

19. (previously presented) The article of claim 16, wherein the etch stop layer has a dielectric constant in a range of less than about 2.8.

20. (previously presented) The article of claim 16, wherein the etch stop layer has a dielectric constant in a range of about 2.

21-27. (canceled)

28. (previously presented) The structure according to claim 1, further comprising:

an electrically conductive trace disposed in the substrate;

a first recess in the ILD layer with a first width and extending from a bottom surface of the ILD layer up to a position partway through the ILD layer;

a second recess in the ILD layer with a second width wider than the first width and extending from the top of the first recess to the top of the ILD layer; and

a contact disposed in the first and second recesses, wherein the contact makes an electrical connection to the trace.

29. (previously presented) The structure according to claim 1, wherein:

the ILD layer has a third thickness; and

the third thickness is greater than the second thickness.

30. (previously presented) The structure according to claim 1, wherein:

the ILD layer has a third thickness; and

the third thickness is at least about 5 times as thick as the second thickness.

31. (previously presented) The structure according to claim 1, wherein the second thickness is greater than the first thickness.

32. (previously presented) The structure according to claim 1, wherein the second thickness is at least about 10 times as thick as the first thickness.

33. (previously presented) The structure according to claim 1, wherein:

the ILD layer has a third thickness;

the third thickness is at least about 5 times as thick as the second thickness; and

the second thickness is at least about 10 times as thick as the first thickness.

34. (previously presented) The structure according to claim 1, wherein:

the diffusion barrier layer comprises silicon nitride;

the etch stop layer comprises an organic polymer;

the ILD layer comprises a carbon doped oxide and has a third thickness;

the third thickness is at least about 5 times as thick as the second thickness; and

the second thickness is at least about 10 times as thick as the first thickness.

35. – 38. (canceled)